UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,999	12/03/2003	Witold P. Maszara	H1855	7143

22898 7590 03/21/2005

THE LAW OFFICES OF MIKIO ISHIMARU
1110 SUNNYVALE-SARATOGA ROAD
SUITE A1
SUNNYVALE, CA 94087

EXAMINER	
TRAN, MAI HUONG C	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,999	MASZARA, WITOLD P.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *1-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/3/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Applicant's election with traverse of Group I (claims 13-20) drawn to a semiconductor device is acknowledged. Accordingly, claims 1-12 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Because Applicant did not distinctly and specifically point out the supposed error in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

The traversal is on the ground(s) that see the election paper. This is not found persuasive because the fields of search for method' and device claims are NOT coextensive and the determinations of patentability of method and device claims are different, that is process limitations and device limitations are given weight differently in determining the patentablitity of the claimed inventions. Also, the strategies for doing text searching of the device claims and method claims are different. Thus, separate searches are required.

The requirement is still deemed proper and is therefore made **FINAL**.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 13-20 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,812,527 to Dennard et al.

Regarding to claim 13, Dennard discloses a device comprising a semiconductor substrate (col. 3, lines 1-10); a gate dielectric 40 on the semiconductor substrate; a gate 42 on the gate dielectric 40; a sidewall spacer 48 on the semiconductor substrate adjacent the gate and the gate dielectric; an epitaxial thickening layer 52 on the semiconductor substrate adjacent the sidewall spacer 48; silicide layers 56 in at least a portion of the epitaxial thickening layer; source/drain regions 50, beneath the silicide layers 56, that are enriched with dopant from the silicide layers; a dielectric layer 58 over the silicide layers 56; and contacts 60 in the dielectric layer 58 to the silicide layers 56 (col. 3, cols 7-8, and figs. 1, 14, 15).

Regarding to claim 14, Dennard discloses the device wherein the epitaxial thickening layer and the adjacent top of the semiconductor substrate are dopant implanted regions (col. 7, lines 1-5).

Regarding to claim 15, the device wherein the silicide layers in the epitaxial thickening layer further comprise silicide layers formed by thermal silicidation of deposited metallic layers into a dopant implanted epitaxial thickening layer (col. 8, lines 22-26).

Regarding to claim 16, the device wherein the source/drain regions 50 that are enriched with dopant from the silicide layers have a dopant profile that is steeper than the profile of dopant lacking enrichment from the silicide layers (col. 7, lines 65-67).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16-20 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,812,527 to Dennard et al. in view of Sitaram et al. (5,352,631) and further in view of the remark.

Regarding to claim 16, Dennard discloses the claimed invention except for the device wherein the source/drain region are enriched with dopant from the silicide layers having a dopant profile that is steeper than the profile of dopant lacking enrichment from the silicide layers.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device wherein the source/drain region are enriched with dopant from the silicide layers having a dopant profile that is steeper than the profile of dopant lacking enrichment from the silicide layers.

Regarding to claim 17, Dennard discloses the claimed invention except for the device wherein the dopant is a material selected from a group consisting of arsenic, phosphorus, antimony, boron, indium, and a combination thereof. However, Sitaram teaches the dopant is a material selected from a group consisting of arsenic, phosphorus, antimony, boron, indium, and a combination thereof (col. 6, lines 1-4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dopant that is a material selected from a group consisting of arsenic, phosphorus, antimony, boron, indium, and a combination thereof, as taught by

Sitaram in order to prevent resistive contacts and interconnects that are not desirable for electrical circuits due to the fact that resistance limits maximum current flow, may create heat, and may result in reduced circuit accuracy, consistency, and performance (col. 1, lines 15-19).

Regarding to claim 18, Dennard discloses the claimed invention except for the device wherein the silicide layers are a silicide of a metal selected from a group consisting of cobalt, nickel, titanium, hafnium, platinum, and a combination thereof. However, Sitaram teaches the silicide layers are a silicide of a metal selected from a group consisting of cobalt, nickel, titanium, hafnium, platinum, and a combination thereof (col. 1, lines 26-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the silicide layers that are a silicide of a metal selected from a group consisting of cobalt, nickel, titanium, hafnium, platinum, and a combination thereof, as taught by Sitaram in order to prevent resistive contacts and interconnects that are not desirable for electrical circuits due to the fact that resistance limits maximum current flow, may create heat, and may result in reduced circuit accuracy, consistency, and performance (col. 1, lines 15-19).

Regarding to claim 19, Dennard discloses a device comprising a semiconductor substrate (col. 3, lines 1-10); a gate dielectric 40 on the semiconductor substrate; a gate

42 on the gate dielectric 40; a sidewall spacer 48 on the semiconductor substrate adjacent the gate and the gate dielectric; an epitaxial silicon thickening layer 52 on the surface of the semiconductor substrate adjacent the sidewall spacer 48 and the gate 42, the epitaxial thickening layer and the adjacent top of the semiconductor substrate being dopant implanted regions (col. 7, lines 1-5); silicide layers 56 in at least a portion of the epitaxial silicon thickening layer; source/drain regions 50, beneath the silicide layers 56, that are enriched with dopant, from the silicide layers; a silicide layer 54 on the gate 42; a dielectric layer 58 over the silicide layers 54, 56; and contacts 60 in the dielectric layer 58 to the silicide layers 54, 56 (cols 7-8 and figs. 1, 14, 15).

However, Dennard does not disclose the source/drain regions that has a dopant profile that is steeper than the profile of dopant lacking enrichment from the silicide layers; the dopant being a material selected from a group consisting of arsenic, phosphorus, antimony, boron, indium, and a combination thereof; the silicide layers being a silicide of a metal selected from a group consisting of cobalt, nickel, titanium, hafnium, platinum and a combination thereof.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device wherein the source/drain region are enriched with dopant from the silicide layers having a dopant profile that is steeper than the profile of dopant lacking enrichment from the silicide layers.

Sitaram teaches the dopant is a material selected from a group consisting of arsenic, phosphorus, antimony, boron, indium, and a combination thereof (col. 6, lines 1-

4), the silicide layers are a silicide of a metal selected from a group consisting of cobalt, nickel, titanium, hafnium, platinum, and a combination thereof (col. 1, lines 26-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dopant is a material selected from a group consisting of arsenic, phosphorus, antimony, boron, indium, and a combination thereof and the silicide layers are a silicide of a metal selected from a group consisting of cobalt, nickel, titanium, hafnium, platinum, and a combination thereof, as taught by Sitaram in order to prevent resistive contacts and interconnects that are not desirable for electrical circuits due to the fact that resistance limits maximum current flow, may create heat, and may result in reduced circuit accuracy, consistency, and performance (col. 1, lines 15-19).

Regarding to claim 20, Dennard discloses the device wherein the silicide layers in the epitaxial silicon thickening layer further comprise silicide layers formed by thermal silicidation of deposited metallic layers into a dopant implanted epitaxial silicon thickening layer (col. 7, lines 1-5).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mai-Huong Tran whose telephone number is (571)272-1796. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mai-Huong Tran
Examiner
Art Unit 2818